UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/706,968	11/14/2003	Jeffrey T. Wetzel	244051US6YA	7489

22850 7590 07/31/2006

C. IRVIN MCCLELLAND
OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C.
1940 DUKE STREET
ALEXANDRIA, VA 22314

EXAMINER	
LUU, CHUONG A	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 07/31/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/706,968	WETZEL ET AL.	
	Examiner	Art Unit	
	Chuong A. Luu	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *16-19 and 22-40* is/are pending in the application.

4a) Of the above claim(s) *23-35* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *16-19, 22 and 36-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments with respect to claims 16-19, 22 and 36-40 have been considered but are moot in view of the new ground(s) of rejection.

PRIOR ART REJECTIONS

Statutory Basis

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The Rejections

Claims 16 and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Liao (U.S. 6,350,682 B1) in view of Wise et al. (U.S. 6,903,023 B2).

Regarding claim 16, Liao (shown in Figures. 2A-2D) discloses a process for fabricating dual damascene structure comprising: forming a layer of dielectric material (204, 206) on a substrate 200 (see column 2, lines 32-36); forming a hard mask layer (208) on the layer of dielectric material (204, 206) (see column 2, lines 39-41); and forming a dual damascene structure for a metal interconnects (see Figure 2D, column 3, lines 20-25), the dual damascene structure having a bottom opening (216) extending to

a surface of the substrate (200), and a top opening (216) in communication with and wider than the bottom opening (216) and extending to the hard mask layer (208), wherein the hard mask layer (208) is etched to a width of the top opening (216) and used as at least one of a lithographic structure for the formation of the interconnect structure (218), a hard mask, an anti-reflective coating, or a chemical mechanical polishing (CMP) stop layer (see column 3, lines 24-26. Figure 2D).

Regarding claim 39, as discussed in claim 16 above, Liao (seeFigures. 2A-2D) discloses the fabrication of the dual damascene structure comprises first etching the hard mask layer (208) to the width of the bottom layer, and then etching the hard mask layer (208) to the width of the top layer.

Liao teaches the above outlined features except for disclosing the hard mask layer (208) is made of TERA material. However, Wise discloses a method for removing carbon from or stripping a TERA layer having a layer of tunable etch resistant anti-reflective (TERA) material (26) as a hard-mask (see column 3, lines 25-63 and column 4, lines 3-10) on the layer of dielectric material (22, 24). Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to modify the process of Liao by using TERA as a material for the hard-mask layer (208) because such a TERA layer would provide anti-reflective coating for DUV lithography, as taught by Wise (see column 3, lines 59-61). Doing so would facilitate the manufacture of the semiconductor device and to avoid damage oxide or nitride layers under the TERA film and also provide good selectivity.

Claims 17-19, 22, 36-38 and 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Liao (U.S. 6,350,682 B1) in view of Wise et al. (U.S. 6,903,023 B2) and further in view of Gaillard et al. (U.S. Pat. 6,500,773) of record.

Liao and Wise teach everything above except for specifically describing a step of forming a layer of light-sensitive material on the layer of TERA material, wherein the optical properties of the light-sensitive layer. Furthermore, Gaillard teaches an integrated circuit fabrication process having a layer of tunable etch resistant anti-reflective (TERA) material as following

Regarding claims 17-18, Gaillard (Figs. 3D and 4D) further discloses a step of forming a layer of light-sensitive material (408/304) on the layer of TERA material (404/302), wherein the optical properties of the light-sensitive layer (408/304) and the TERA layer (404/302) are inherently substantially the same because both of the light-sensitive layer (408/304) and the TERA layer (404/302) have the same wavelength less than about 250nm (column 2, lines 13-24); and exposing the layer of light-sensitive material (408/304) to a pattern of radiation, wherein the forming the layer of TERA material (404/302) facilitates producing a pattern in the layer of light-sensitive material (408/304) substantially the same as the pattern of radiation; wherein the forming the layer of TERA material comprises providing a part of the lithographic structure for the formation of a metal interconnect for the device structure (figures 3D and 4D, column 2, lines 8-28, column 8, lines 18-26 and column 9, lines 27-29).

Regarding claim 19, Gaillard discloses wherein the forming the layer of TERA material comprises depositing the layer of TERA material using at least one of plasma enhanced CVD (column 4, lines 34-35).

Regarding claim 22, Gaillard (Figs. 3D and 4D) discloses wherein the forming a damascene structure comprises integrating a tunable anti-reflective coating with a dual damascene structure formed using a method comprising at least one a via-first method, a full-via-first method, a full-via with no stop layer method, a trench-first method, and a buried via mask method.

Regarding claims 36-38, Gaillard (Fig. 4D) discloses a step of forming a damascene structure comprises using the layer of TERA material 404 as a hard mask, a sacrificial layer or a CMP stop layer for forming the top opening of the dual damascene structure.

Regarding claim 40, Gaillard (Fig. 5E) discloses a step of forming another layer of TERA material 504 in the layer of dielectric material (502,508); and etching the another layer to a width of the bottom opening.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to modify the process of Liao and Wise .Doing so would facilitate the manufacture of the semiconductor device and enhance the speed of the dual damascene.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chuong A. Luu whose telephone number is (571) 272-1902. The examiner can normally be reached on M-F (6:15-2:45).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Chuong Anh Luu
Patent Examiner
July 20, 2006